BP85256D
Ultra-high Integration Off-line Switcher IC

Description

The BP85256D is a high performance, highly integrated power supply switcher IC with low standby consumption. The BP85256D can be configured as buck, buck-boost topologies for universal 85~265V AC inputs.

The BP85256D integrates a 650 V power MOSFET, a high-voltage current source for self-biasing, a current sensing circuit, an output feedback circuit, a freewheeling diode and a controller. External VCC capacitor and loop compensation components can be eliminated, which reduces cost and size of overall power systems, and improves reliability.

The BP85256D employs multi-mode control algorithm. As a result, the no-load power consumption and the average efficiency have been improved, and the audible noise is reduced.

The BP85256D features comprehensive protections, including short circuit protection (SCP), output over voltage protection (OVP), over load protection (OLP), FB open loop protection, cycle-by-cycle current limit, and over temperature protection (OTP).

The BP85256D is available in SOP-7 package.

SOP-7 package

Features

- Integrated VCC capacitor, freewheeling diode and feedback diode
- Integrated 650V power MOSFET
- Integrated high-voltage current source for self-biasing
- No load consumption <50mW at 230VAC
- Fixed 12V output
- Fast transient response and low output ripple
- Optimized line and load regulation
- Reduced audible noise at light load
- Adaptive switching frequency, 45kHz maximum
- Frequency modulation for EMI improvement
- Internal soft start
- Comprehensive protections
  - Short circuit protection (SCP)
  - Over voltage protection (OVP)
  - Over load protection (OLP)
  - Open loop protection
  - Cycle-by-cycle current limit
  - Over temperature protection (OTP)

Applications

- Home appliances
- Motor driver standby power
- IoT, smart home, smart LED drivers

Typical Application

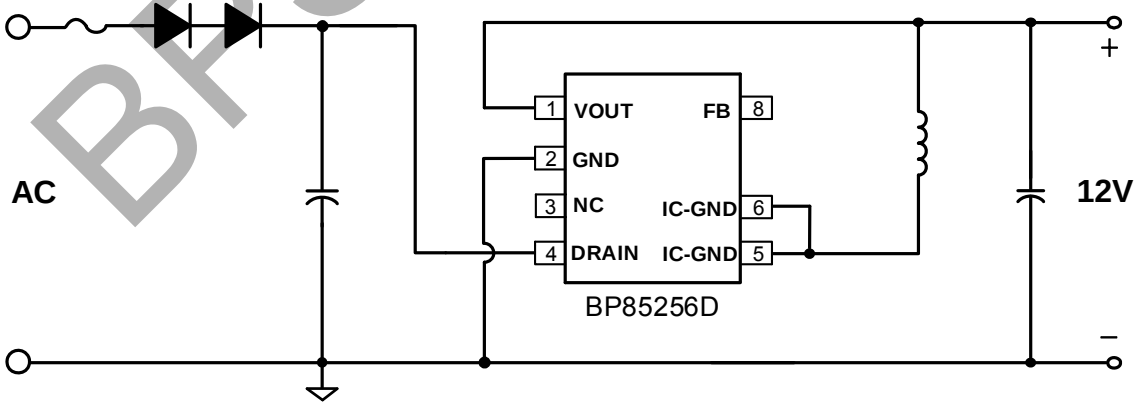


Figure 1. Typical buck application with the BP85256D

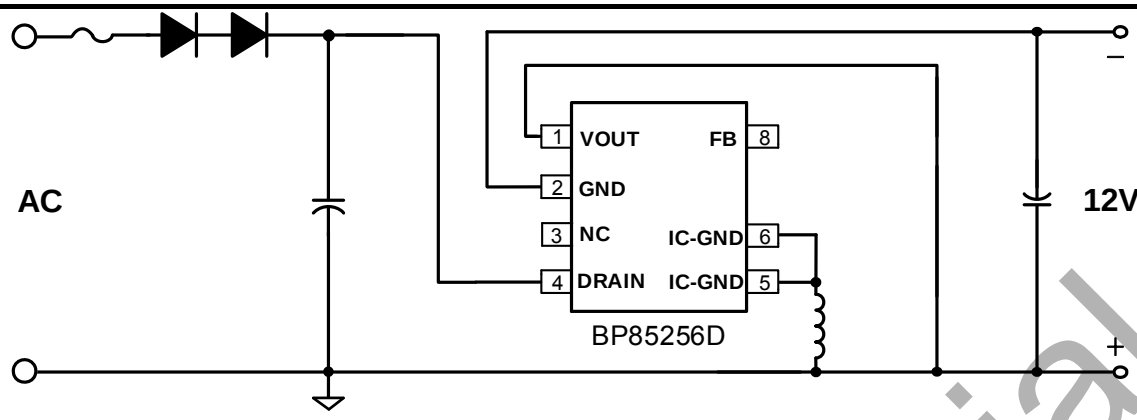


Figure 2. Typical buck-boost application with the BP85256D

Ordering Information

Part Number	Package	Packing	Marking
BP85256D	SOP-7	Tape & Reel 4,000 pcs/Reel	BP85256 XXXXXYY ZZWWD

Pin Configuration and Marking Information

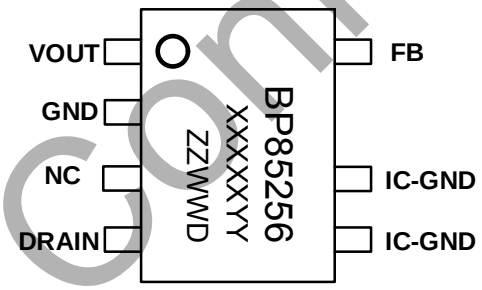


Figure 3. SOP-7 pin configuration

BP85256：Part number
XXXXXYY: Lot code
ZZ: Internal code
WW：Week code
D：Package type(D:SOP)

Pin Functions

Pin NO.	Pin Name	Description
1	VOUT	Output voltage pin. Anode of the internal feedback diode.
2	GND	Ground reference for the output voltage. Anode of the internal freewheeling diode.
3	NC	Not connected.
4	DRAIN	Drain connection of the internal power MOSFET. Input of the high-voltage current source.
5、6	IC-GND	Ground reference for the IC. Source connection of the internal power MOSFET. Cathode of the internal freewheeling diode.
8	FB	Voltage feedback pin. Cathode of the internal feedback diode. No external connection required.

Recommended Output Current (Note 1)

Part NO.	Output voltage(V)	Continuous output current(mA)	Pulsed output current(mA)
BP85256D	12	300	350

Note 1:

The continuous output current is tested in semi-enclosed frame of 75 °C (Buck/Buck-Boost), continuous working time > 2 hours.

The pulsed output current is tested in semi-enclosed frame of 75 °C (Buck/Buck-Boost), continuous working time > 1 minute.

Absolute Maximum Ratings (Note 2)

(T_A=25°C, , unless otherwise noted)

Symbol	Parameter	Value	Units
V_{DRAIN}	Drain to source voltage	-0.3~650	V
V_{FB}	FB to IC-GND voltage	-0.3~30	V
V_{GND}	GND to IC-GND voltage	-650~ 0.3	V
V_{OUT}	VOUT to IC-GND voltage	-650~ 30	V
P_{DMAX}	Continuous power dissipation (Note 3)	0.97	W
θ_{JA}	Junction-to-ambient thermal resistance (Note 4)	129	°C/W
θ_{JC}	Junction-to-case thermal resistance (Note 4)	70	°C/W
T_J	Operating junction temperature	-40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C
ESD	ESD capability, human body mode (Note 5)	3.5	kV

Note 2: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. The electrical characteristics table defines the operation range of the device, and the electrical characteristics is assured on DC and AC voltage by test program. For the parameters without minimum and maximum value in the EC table, the typical value defines the operation range, but the accuracy is not guaranteed by spec.

Note 3: The maximum power dissipation decreases if temperature rises. It is decided by T_{JMAX}, θ_{JA}, and environment temperature (T_A). The maximum power dissipation is the lower one between $P_{DMAX} = (T_{JMAX} - T_A)/ \theta_{JA}$ and the number listed in the maximum table.

Note 4: 1 in.^2, 2-layrer PCB, follow JEDEC standard.

Note 5: 1.5kΩ in series with 100pF, follow JEDEC standard.

Electrical Characteristics (Note 6) (T_A=25°C, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Self-powered						
V_{DS_SUP}	Minimum drain voltage for start-up			40		V
I_{CC}	Operation current	V_{DRAIN}=40V		100		uA
I_Q	Quiescent current	V_{DRAIN}=11V		80	110	uA
Feedback						
V_{FB}	FB modulation voltage		12.15	12.45	12.75	V
V_{FB_OLP}	FB OLP threshold			6.4		V
t_{OLP}	OLP delay time			1024		cycles
V_{FB_SC}	FB SCP threshold			2.3		V
t_{SC}	SCP delay time			256		cycles
V_{FB_OVP}	FB OLP threshold			15.5		V
t_{AR_OFF}	OLP delay time			0.5		s
Oscillator						
f_{S_MAX}	Maximum switching frequency		40	45	50	kHz
f_{S_MIN}	Minimum switching frequency			0.5		kHz
t_{ON_MAX}	Maximum turn-on time		8			us
Current Sense						
I_{LIMIT_MAX}	Maximum peak current limit		540	600	660	mA
I_{LIMIT_MIN}	Minimum peak current limit			180		mA
t_{LEB}	Leading edge blanking			240		ns
Internal MOSFET						
R_{DS_ON}	On-state resistance	I_{DS}=50mA		11	15	Ω
I_{DSS}	MOSFET OFF-state leakage current	V_{DS}=500V		10		uA
I_{DSS2}	DRAIN pin OFF-state leakage current	V_{DS}=650V, V_{FB}=19.5V		110		uA
BV_{DSS}	Breakdown voltage		650			V
Internal Freewheeling Diode						
V_{RRM1}	Maximum reverse breakdown voltage	I_R=5uA	650			V
V_{F1}	Forward voltage	I_F=500mA		1.2	1.8	V
I_{FAV1}	Maximum average rectified forward current		500			mA

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
T_{RR1}	Reverse recovery time	I_F=300mA, I_R=1.0A, I_{RR}=150mA			35	ns
Internal Feedback Diode						
V_{RRM2}	Maximum reverse breakdown voltage	I_R=5uA	650			V
V_{F2}	Forward voltage	I_F=2mA		0.58	0.65	V
I_{FAV2}	Max. average rectified forward current		500			mA
T_{RR2}	Reverse recovery Time	I_F=300mA, I_R=0.6A, I_{RR}=150mA			35	ns
Thermal shutdown						
T_{OTP}	Thermal shutdown temperature			145		°C
T_{HYST}	Thermal shutdown hysteresis			40		°C

Note 6: *The maximum and minimum parameters specified are guaranteed by test, the typical values are guaranteed by design, characterization and statistical analysis. The IC-GND is used as voltage reference unless otherwise noted*

Functional Block Diagram

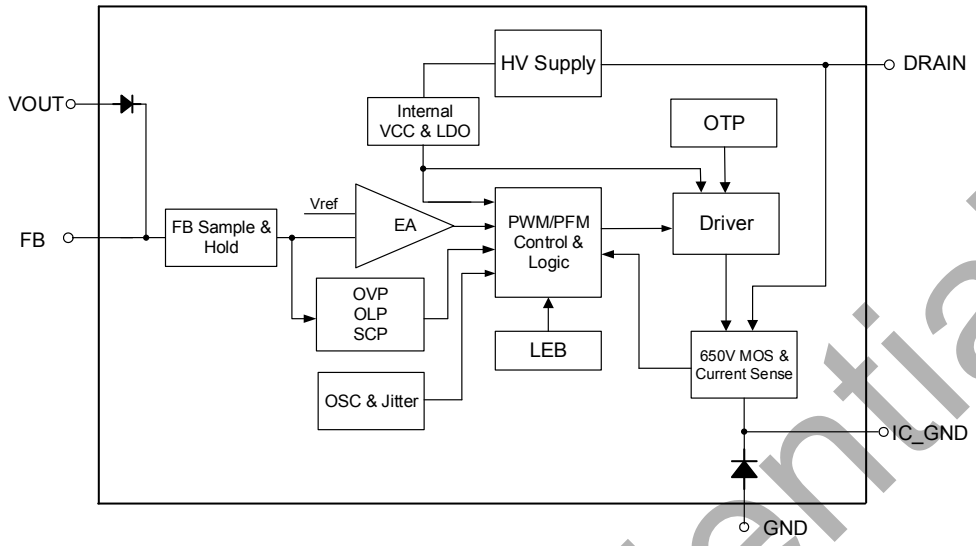


Figure 4. Functional block diagram

Functional Description

BP85256D is an off-line switching regulator for universal line input and 12V fixed output voltage applications. It adopts multi-mode control algorithm and loop compensation technique to reduce the external components. BP85256D integrates a 650V power MOSFET, a freewheeling diode, a high voltage current source, a current sensing circuit, a voltage feedback circuit and a suite of protections. Good performance has been achieved without VCC capacitor, nor loop compensation component. The switching frequency and peak current limit are adjusted automatically according to the load conditions. Meanwhile, low no-load consumption, small output ripple, good transient response, and unnoticeable audible noise make BP85256D suitable for non-isolated auxiliary power supply.

*(**Note 7:** All of the parameters used in these descriptions are typical values, unless they are specified as minimum or maximum.)*

Start-up Operation

The BP85256D integrates a high-voltage current source, no need for external VCC capacitance. When the AC input becomes available, the bulk capacitor voltage rises. The high-voltage current source is activated and starts to charge the internal VCC capacitor through the DRAIN pin. The BP85256D starts switching as soon as the internal VCC voltage reaches 11V. When the internal VCC voltage drops below 5V, the BP85256D turns off the internal MOSFET. The high-voltage current source charges the internal VCC capacitor through the DRAIN pin during the MOSFET is turned off.

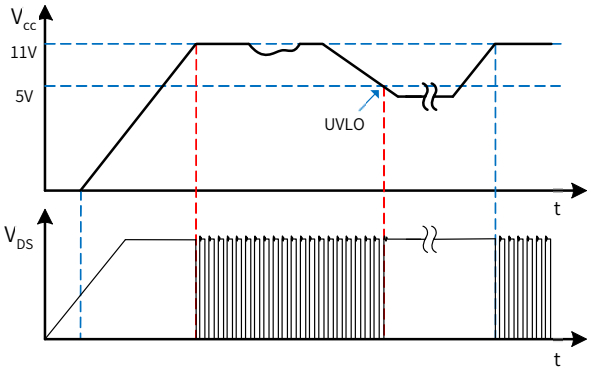


Figure 5. Internal VCC Start-up and UVLO

Soft Start

The BP85256D features a soft start to increase the peak current of the power MOSFET (current limit) gradually during a power-up or restart phase. Because the output voltage is low during start-up, the inductor demagnetization is very slow, and the system operates in deep CCM. Therefore, the reverse recovery current of the freewheeling diode is large, which may lead to more

power dissipation on the power MOSFET, even destroy the power MOSFET. The internal soft start circuit increases the MOSFET peak current gradually, so does the reverse recovery current of the freewheeling diode. During the soft start process (Figure 6), the initial current limit is 50% of the maximum current limit, and it is increased to 75% of that after 32 switching cycles. After 32 switching cycles, the soft start process is completed, and the current limit returns to the maximum value.

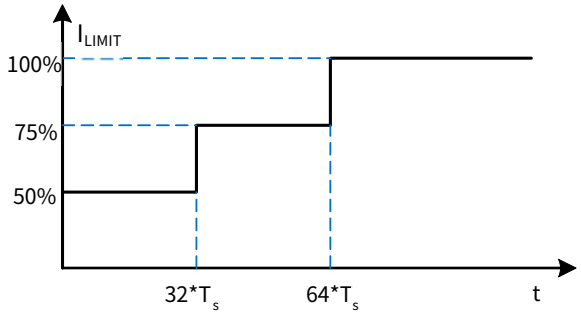


Figure 6. Soft start

Output Voltage Feedback

The VOUT pin samples the output voltage to FB pin via an internal feedback diode. The voltage of the FB pin is scaled by the resistor divider, and then is compared with an internal reference voltage. The difference between the two voltages is amplified by an error amplifier (EA) and the EA output controls the current limit and switching frequency to regulate the output voltage. The output voltage sampling is performed only at the third microseconds during the freewheeling state. It is recommended to ensure that the freewheeling time is greater than 7us to prevent abnormal operation caused by false feedback.

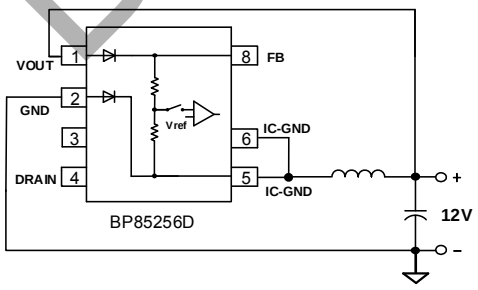


Figure 7. Output voltage feedback network

Multi-mode Control

The BP85256D adopts PWM/PFM multi-mode control algorithm. As a result, the system' s no-load power consumption is reduced, average efficiency is improved, and light load audible noise is eliminated. As shown in Figure 8, at full load, the BP85256D operates in PFM mode, the current limit of the power MOSFET is set to its maximum value (I_{LIMIT_MAX}), and the switching frequency increases as the load increases. The maximum switching frequency is f_{S_MAX} (45kHz). When load reduces, the current limit value starts to decrease once the switching frequency drops to 22KHz. The switching frequency will be kept at 22 kHz and the BP85256D operates in the PWM mode, until the minimum current limit (I_{LIMIT_MIN}) is reached. Under lighter load conditions, the BP85256D goes into the PFM mode again, and the switching frequency decreases further towards the minimum value f_{S_MIN} (0.5KHz). Reduced inductor current results in a low flux density during light load and No load, therefore the audible noise is eliminated.

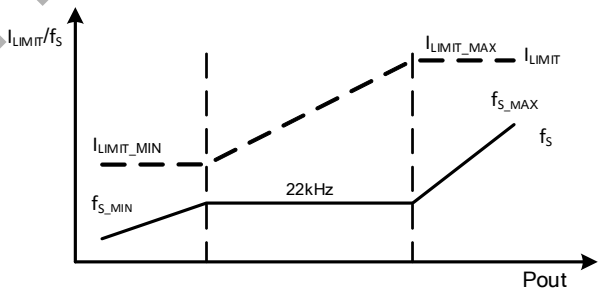


Figure 8. Multi-mode control

Current Sense

The BP85256D integrates a current sensing circuit to limit the peak current of the power MOSFET cycle by cycle for current mode control without external current sensing resistor. The on time of the power MOSFET is determined by the peak current limit mechanism. In order to avoid the premature termination of the switching pulse due to the parasitic capacitance and the diode' s reverse recovery time, an internal leading edge blanking (LEB) circuit has been employed to inhibit the current limiting comparator for a short time (t_{LEB}).

Auto-restart

When a fault condition, such as output short circuit, output overload or output over voltage, the protections will be triggered, the BP85256D will stop operation and the power MOSFET will be turned off for t_{AR_OFF} (0.5s). The auto-restart circuit alternately enables and disables the switching of the power MOSFET until the fault condition is removed. Each auto-restart will undergo a soft start procedure.

Short Circuit/Over Load Protection

The BP85256D detects output faults through the FB pin. The short circuit protection (SCP) will be triggered if the FB pin voltage is below V_{FB_SC} (2.3V) for t_{SC} (256 Cycles). The over load protection (OLP) will be triggered if the FB voltage is lower than V_{FB_OLP} (6.4V) for t_{OLP} (1024 Cycles). As soon as these two faults disappear, the power supply resumes operation with an auto-restart process as the one shown in Figure 9.

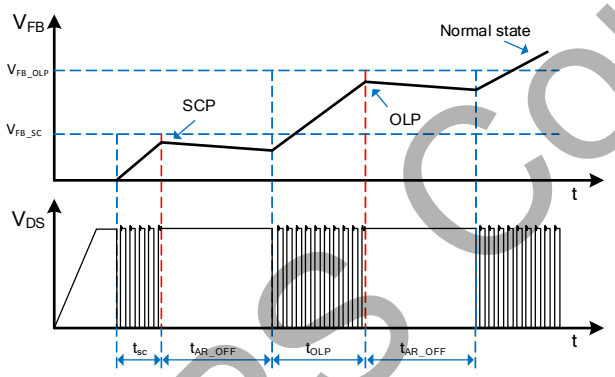


Figure 9. Short protection/ over load protection

Output Over Voltage Protection

The output over voltage protection (OVP) will be triggered with an auto-restart process if the FB pin voltage is above V_{FB_OVP} (15.5V) for 3 switching cycles.

Over Temperature Protection

The threshold for over temperature protection is set at T_{OTP}(145°C) typical with a hysteresis (T_{HYST}, 40°C). When the die temperature rises above this threshold the power MOSFET is disabled and remains disabled until the die temperature falls below (T_{OTP}-T_{HYST}), at which point the power MOSFET is re-enabled. A large hysteresis can prevent overheating.

Application Information

Output Inductor Selection （For Buck）

The BP85256D can operate in CCM or DCM, depending on maximum current limit, output current, switching frequency, and the inductance. If $I_{OUT} > 0.5*I_{LIMIT\_MAX}$, CCM is mandatory to meet the output current requirement. When $I_{OUT} < 0.5*I_{LIMIT\_MAX}$, the conduction mode depends on the inductance which determines the switching frequency. Normally, the converter can deliver more peak power with larger inductance, but the system size and cost get increased. In addition, it will lead to more switching loss in CCM and worsen transient response. On the contrary, small inductance has benefits of small size, low cost, good transient response, but the peak output current is limited. With above discussions, a minimum value of the inductance, required to deliver the specified output power, can be calculated. Therefore, select CCM when $I_{OUT} > 0.5*I_{LIMIT\_MAX}$, otherwise select DCM.

For CCM, as shown in Figure 10, the required minimum inductance can be calculated according to the following equation:

$$L_{MIN} = \frac{(V_{OUT} + V_{Diode}) * (V_{IN} - V_{DS} - V_{OUT})}{(V_{IN} - V_{DS} + V_{Diode}) * f_S * \Delta I_L}$$

Where，V_{IN_MAX} is the maximum DC voltage on the bulk capacitor.

V_{OUT} is the output voltage

V_{Diode} is voltage drop of the freewheeling diode

V_{DS} is the on state drain to source voltage drop

f_S is the switching frequency

t_{ON} is on time of the MOSFET

t_{OFF} is off time of the MOSFET

I_{LIMIT_MAX} is the maximum current limit

$$\Delta I_L = 2 * (I_{LIMIT\_MAX} - I_{OUT})$$

$$V_{DS} = I_{OUT} * R_{ds(ON)}$$

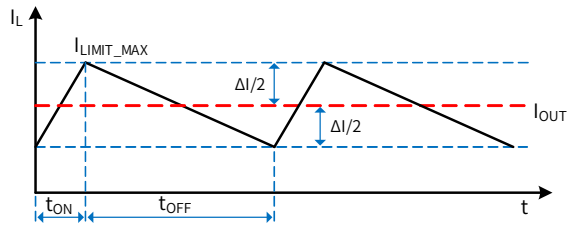


Figure 10. Inductor current in CCM

The RMS value of the inductor current is:

$$I_{RMS} = \sqrt{{I_{LIMIT\_MAX}}^2 - I_{LIMIT_{MAX}} * \Delta I_L + \frac{{\Delta I_L}^2}{3}}$$

For DCM, as shown in Figure 11, the required minimum inductance can be calculated as:

$$L_{MIN} = \frac{2 * I_{OUT} * (V_{OUT} + V_{Diode}) * (V_{IN} - V_{DS} - V_{OUT})}{(V_{IN} - V_{DS} + V_{Diode}) * f_S * I^2_{LIMIT\_MAX}}$$

where,

$$V_{DS} = \frac{1}{2} * I_{LIMIT\_MAX} * R_{ds(ON)}$$

The RMS value of the inductor current is:

$$I_{RMS} = I_{LIMIT\_MAX} * \sqrt{\frac{t_{ON} + t_{OFF}}{3} * f_S}$$

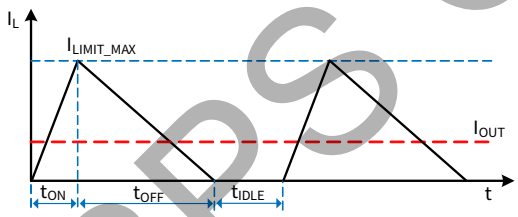


Figure 11. Inductor current in DCM

Generally, to take manufacturing variations into considerations, a tolerance factor (a typical value is 1.15) should be incorporated in the above equations. Furthermore, I_{LIMIT_MAX} should be the lower bound value from the Electrical Characteristics Table.

To further reduce standby power consumption, the BP85256D reduced the dummy load as small as possible by reducing the current limit and the switching frequency at light load conditions. There is a minimum inductance value to prevent the peak current of the power MOSFET exceeding the minimum current limit with the minimum on time.

$$L \geq \frac{t_{LEB} * (V_{IN\_MAX} - V_{OUT})}{I_{LIMIT\_MIN}}$$

Where, t_{LEB} is internal leading edge blanking time, and I_{LIMIT_MIN} is the minimum current limit. As shown in Figure 12, when the inductance gets reduced, the peak current increases, which results in a higher average output current. A large dummy load is thus required to bypass the current.

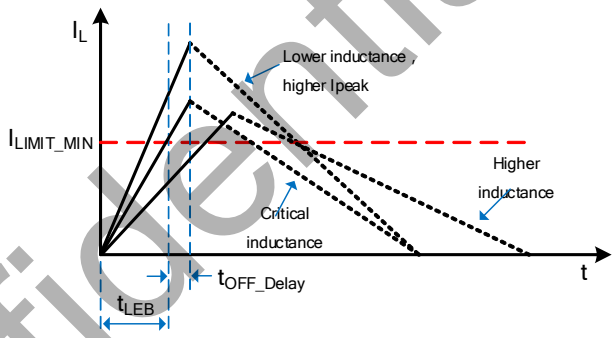


Figure 12. Inductor current at no load

In addition, the selected inductor should ensure that the freewheeling time at the lowest current limit is greater than 7us to ensure the normal feedback sampling,

$$L \geq \frac{V_{OUT} * 7us}{I_{LIMIT\_MIN}}$$

Therefore, the final selected inductance value usually needs to satisfy the above three conditions.

The RMS current rating of the inductor should be checked, and the saturation current should be higher than the maximum current limit I_{LIMIT_MAX}. The RMS current and saturation current of the inductor are generally given in the datasheets of manufacturers.

Input Capacitor Selection

The input capacitor filters the AC ripple voltage and improves the EMI and surge performance. The capacitance should be large enough to make sure that minimum BUS voltage is larger than 70V. With full-wave rectifiers, 3μF/W can be used at 85~265VAC universal AC input. With half-wave rectifiers, the input capacitance is

usually set as 6μF/W for universal AC inputs. The input capacitance could be halved for high line only applications if the EMI and surge requirements can be met.

Output Capacitor Selection

The output capacitor smooths the inductor current and stabilizes the DC output voltage. The output capacitor is normally selected based on the output voltage ripple requirement. The capacitance and ESR of the output capacitor both contribute to the output voltage ripple:

$$\Delta V_{OUT} = \Delta V_{ESR} + \Delta V_C$$

In CCM, the output voltage ripple due to the output capacitor's capacitance is:

$$\Delta V_C = \frac{\Delta I_L}{8 * C_{OUT} * f_S}$$

In DCM, the output voltage ripple due to the output capacitor's capacitance is:

$$\Delta V_C = \frac{I_{OUT} * (I_{LIMIT\_MAX} - I_{OUT})^2}{C_{OUT} * f_S * I_{LIMIT\_MAX}^2}$$

For practical applications, in order to obtain a small ESR, the output capacitance is large, and the output voltage ripple generated by the capacitance is small and can be almost ignored. Therefore, the voltage ripple is mainly generated by the ESR of the capacitor:

$$\Delta V_{ESR} = \Delta I_L * ESR \quad \text{(CCM)}$$

$$\Delta V_{ESR} = I_{LIMIT\_MAX} * ESR \quad \text{(DCM)}$$

Ripple current flowing through the ESR causes power dissipation, which leads to temperature rise inside the output capacitor, especially in DCM when ripple current is larger than CCM. The output capacitance of BP85256D is recommended to be 220uF.

Dummy Load Selection

A dummy load is required to return the inductor current and maintain the output voltage regulation. The dummy load current is equal to the average of the inductor current:

$$I_{AVG} = \frac{1}{2} * I_L * (T_{ON} + T_{OFF}) * f_{S\_MIN}$$

Where, I_L is the peak current at maximum input voltage.

$$I_L = \frac{V_{IN\_MAX}}{L} * t_{Delay} + I_{LIMIT\_MIN}$$

where I_{LIMIT_MIN} is the minimum current limit, t_{Delay} is the turn-off delay time, T_{ON} and T_{OFF} are on and off time of the power MOSFET, respectively.

$$T_{ON} = \frac{L * I_L}{V_{IN\_MAX}}$$

$$T_{OFF} = \frac{L * I_L}{V_{OUT} + V_{Diode}}$$

$$R_L = \frac{V_{OUT}}{I_{AVG}}$$

The calculation takes no account of self-supply current, and the actual dummy load current should be slightly larger. Generally, it is about 1~3mA.

Buck-Boost Applications

BP85256D could be used in buck-boost topology as well to provide negative output voltage with respect to input., As shown in Figure 2, the IC functions similarly as in the buck topology except that the energy is delivered to output only during the off time. the average current through the output inductor are slightly higher in the buck-boost applications than those in the buck ones.

In CCM, the minimum inductance is given by:

$$L_{MIN} = \frac{0.5 * V_{OUT}' * V_{IN}'^2 * \frac{1}{f_S}}{(V_{IN}' + V_{OUT}') * [V_{IN}' * I_{LIMIT\_MAX} - (V_{IN}' + V_{OUT}') * I_{OUT}]}$$

Where,

$$V_{IN}' = V_{IN} - V_{DS}$$

$$V_{OUT}' = V_{OUT} + V_{Diode}$$

$$V_{DS} = \frac{V_{IN}' + V_{OUT}'}{V_{IN}'} * I_{OUT} * R_{ds(ON)}$$

V_{IN} is the input bus voltage

V_{OUT} is the output voltage

I_{OUT} is the output current

V_{Diode} is the forward voltage of freewheel diode

V_{DS} is the on state drain to source voltage

I_{LIMIT_MAX} is the maximum current limit

The RMS inductor current is:

$$I_{RMS} = \sqrt{{I_{LIMIT\_MAX}}^2 - I_{LIMIT_{MAX}} * \Delta I_L + \frac{{\Delta I_L}^2}{3}}$$

Where,

$$\Delta I_L = 2 * (I_{LIMIT_{MAX}} - \frac{I_{OUT}}{V_{IN}'} * (V_{IN}' + V_{OUT}'))$$

In DCM, the minimum inductance is given by:

$$L_{MIN} = \frac{2 * (V_{OUT} + V_{Diode}) * I_{OUT}}{{I_{LIMIT\_MAX}}^2 * f_S}$$

The RMS inductor current is:

$$I_{RMS} = I_{LIMIT\_MAX} * \sqrt{\frac{t_{ON} + t_{OFF}}{3} * f_S}$$

The lower limit of the inductance at light load is the same as the buck applications.

The ripple voltage of the output is dominated by the output capacitor' s ESR:

$$\Delta V_{ESR} = I_{LIMIT\_MAX} * ESR \quad \text{(DCM/CCM)}$$

PCB Layout Guidelines

When designing a PCB for the BP85256D, it is important to follow the guidelines as below:

1) Do not lay copper on the VOUT and FB. And keep the VOUT and FB away from bus voltage, bus ground and output inductance to avoid interference.

2) Laying copper on the IC-GND pin helps to dissipate heat. But too much copper on IC-GND can cause EMI noise. It is recommended to use minimum copper that is required to handle the heat dissipation. To reduce the direct coupling from the switching nodes, the IC-GND should be kept away from AC input lines.

3) The copper on DRAIN can be maximized to improve heat removal as long as the creepage distance is larger than 2mm.

4) The area of power loop should be kept as small as possible. Take the Buck application for example: A loop consists of the bulk capacitor, the integrated MOSFET and the integrated freewheeling diode. The bulk capacitor should be close to the DRAIN to reduce the loop area. Another loop consists of the integrated freewheeling diode, the output inductance and the output capacitance. This area of the loop should also be as small as possible.

5) The inductor may cause interference, therefore, it should be placed far away from FB, VOUT and the AC input lines.

6) To improve the system reliability, the power trace should be wide and short. Such as the trace of bus to GND, GND to output capacitor.

7) The feedback trace should be short for the system reliability.

8) However, due to some objective factors (such as the outline of the PCB), the guidelines 6) and 7) are unable to be followed, a MLCC (100nF) between VOUT pin and GND pin is recommended to improve the system reliability.

Design Example

Figure13 is a design example of BP85256D for universal AC input, 12V/300mA output. A BUCK topology is used.

The input side including RZ1, MOV, CX, D1, D2, EC1, EC2, L1. The RZ1 is a fuse resistor which acts as a fuse and limits the surge current through D1 and D2. The MOV is a metal oxide varistor to protect the system when the surge inputting. CX is a X capacitor. D1, D2 are rectifier diodes, series to double the breakdown voltage. The L1, EC1, EC2 constitute a π filter. The output Inductor, L2 is 1mH(10*14mm). The output capacitor, EC3 is 220uF/16V. The dummy load, R3 is 8.2KΩ.

The power MOSFET, freewheeling diode and the feedback circuit are integrated in BP85256D.

Figure 14 is the PCB layout, a single sided board following the PCB Layout Guidelines.

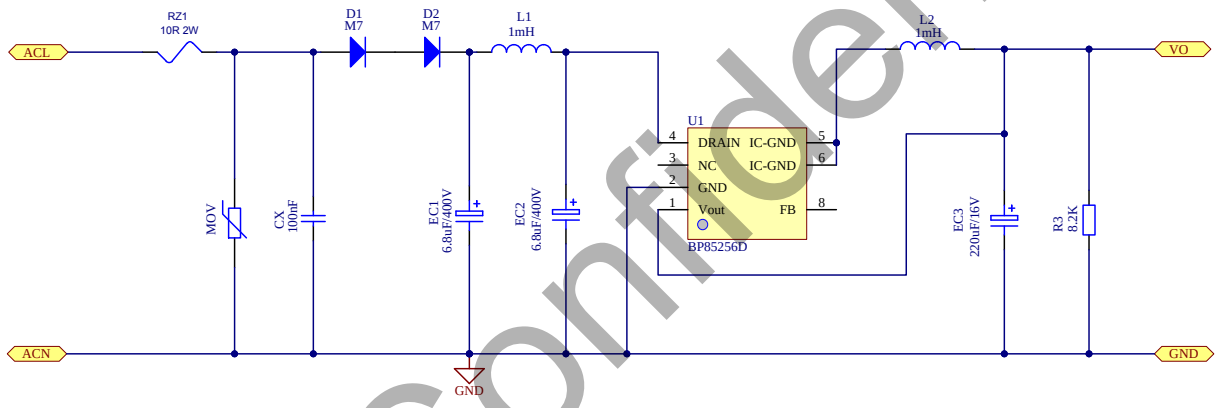


Figure13. BP85256D Design Example, schematic

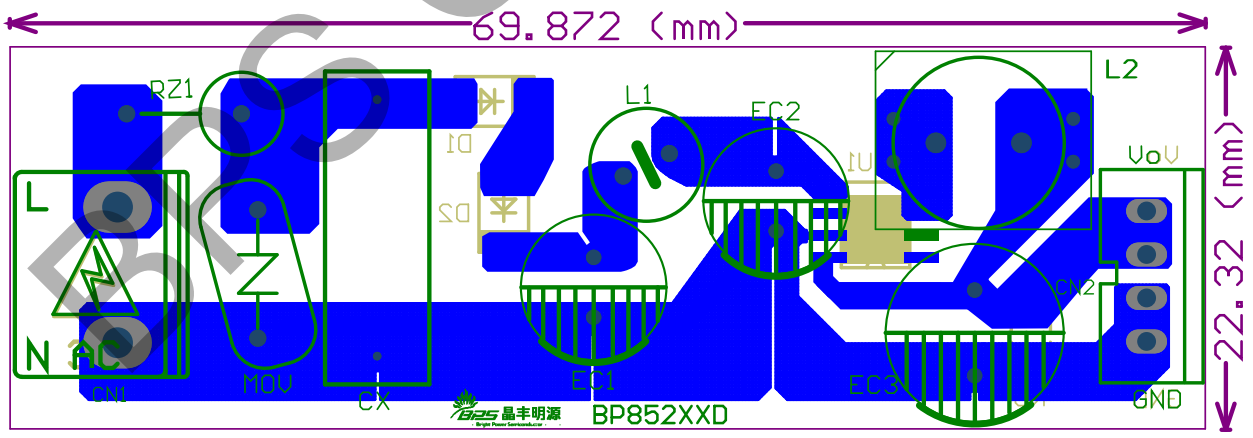
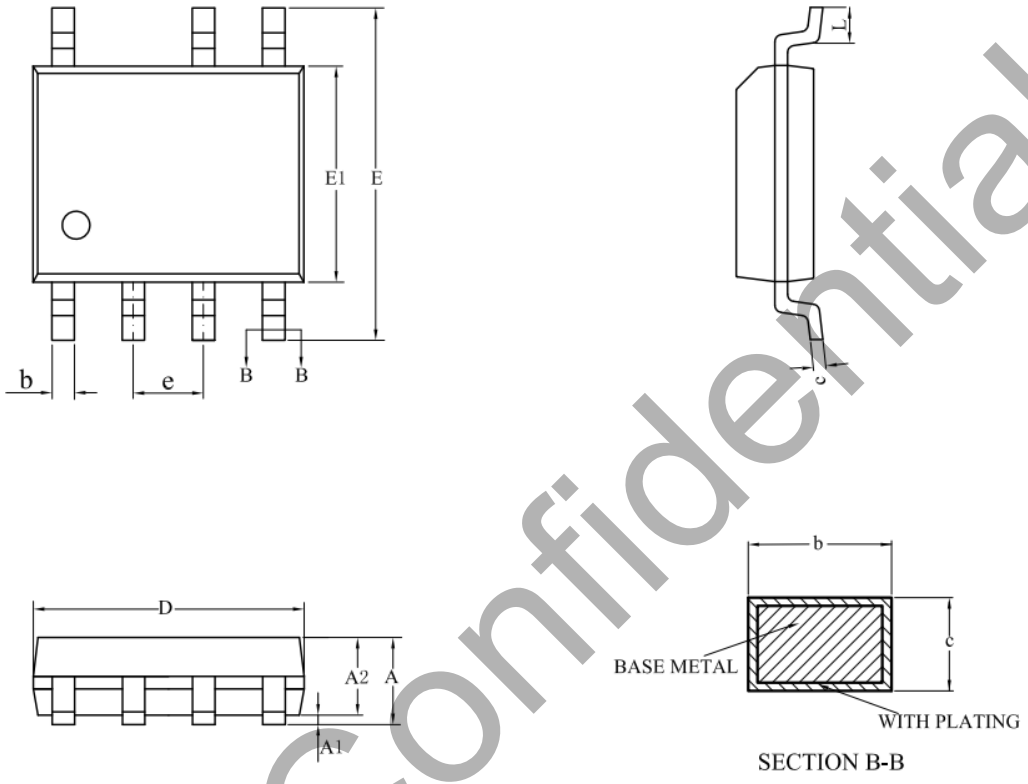


Figure 14. BP85256D Design Example, PCB Layout (single sided)

Package Information

SOP-7 Package Outline



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.30	—	1.80
A1	0.04	—	0.25
A2	1.25	—	1.65
b	0.33	—	0.51
c	0.17	—	0.25
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
L	0.40	—	1.00

Version Information

Revision	Date	Notes
Rev.1.0	8/2022	Initial release
Rev.1.1	9/2022	Update the PCB Layout Guidelines

Disclaimer

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